REMARKS

Claims 1-14 stand rejected, with claims 15-37 withdrawn from consideration. Claims 1-14 have been amended and newly written claims 38-50 are submitted for consideration. Therefore, claims 1-50 remain in this application.

Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

The Examiner's notification that the drawings filed November 8, 2001 are accepted is very much appreciated. Additionally, the Examiner's consideration of the Information Disclosure Statement previously submitted by applicants is very much appreciated.

Applicants query the Examiner's failure to acknowledge applicants' claim for priority contained in the cover sheet of this application when filed on August 8, 2001. Applicants will submit a certified copy of the priority document in due course.

Claims 1 and 7 stand rejected under 35 USC §102(e) as being anticipated by Sahara or Lee. Applicants have amended claim 1 to be directed to a PN type photodiode detector and has added newly written claims 38-50 directed to a PIN photodiode detector, whereas the original claim 1 covered both PN and PIN photodiode detectors in the alternative.

Central to applicants' originally submitted claim is the recitation of a "guard ring delimiting the photodiode detector." This feature has been maintained in

applicants' amended and newly written independent claims which clarify that it actually "surrounds" the photodiode detector. It is this "delimiting" and "surrounding" aspect which accomplishes the beneficial results.

Turning to the Sahara reference, the Examiner cites Figure 13B labeled as "prior art" as disclosing the claimed invention. Applicants note that the Sahara reference contains no teaching of any "guard ring" in spite of the Examiner's labeling item 165B as such. While Sahara calls the structure 165B a "guard ring" in his specification, it clearly does not surround the photodiode portion of the structure (item 165B is a "C"-shaped structure in plan view as seen in Figure 13A and does not extend all the way to the corresponding opposite structure on the other side).

Applicants have clarified that the claimed guard ring not only delimits the photodiode detector, but also surrounds it, thereby clearly distinguishing the Sahara discussion.

Moreover, the Examiner is believed to have misinterpreted the Sahara reference in his citation of Figure 13B and the discussion at column 23, lines 47 and 48. Figure 13B, as noted in Sahara, is prior art, whereas the discussion at column 23, lines 47 and 48 is directed towards "the present invention." To the extent the Examiner is somehow combining Sahara's discussion of prior art and the separate disclosure of Sahara's invention, the Examiner's characterization is believed to be incorrect.

Additionally, applicants' claims recite "at least one epitaxial layer," both as originally filed and as currently amended and such is not present in the Sahara Figure 13A or B. While Figure 13B does disclose epitaxial layer 161, the Examiner suggests that area 164A and B is the epitaxial layer referred to in applicants' claims. It will be readily apparent that areas 164A and B in the Sahara "prior art" are "p-type layers" which are created not by the deposition of an epitaxial layer, but rather by a diffused region and such difference is readily apparent to those having ordinary skill in this field.

Should the Examiner still maintain that area 164 in the Sahara reference comprises applicants' claimed epilayer, he is respectfully requested to point out how or where there is any disclosure in Sahara which supports the contention that section 164 is an epitaxial layer, rather than a diffused region in epilayer 161.

The Examiner also suggests that claim 7 is somehow anticipated by Figure 13B in the Sahara reference. Applicants note that claim 7, dependent from claim 1, specifies that the elements of claim 1 are "arranged to provide a logarithmic response to incident radiation." The old adage of "saying something is so doesn't make it true" would appear to apply here. Merely stating that Sahara discloses such an arrangement does not make it true. The Examiner has pointed to nothing in the Sahara reference which provides any logarithmic response. In fact, 13B shows a conventional avalanche photodiode with no external circuitry such as a logarithmic series load which would confer the claimed logarithmic

characteristics. Moreover, there is no disclosure anywhere that there is a mention of a logarithmic response or circuitry in the Sahara reference.

In view of the above, Sahara fails to disclose structures positively recited in applicants' independent claim 1 and claim 7 and therefore any further rejection thereunder is respectfully traversed.

Similarly to the Sahara reference, the Examiner suggests that Lee discloses in Figure 2 applicants' claimed photodetector circuit. In fact, Lee shows a conventional photodiode using substrate 2 and epilayer 4 grown on the substrate. The Examiner is referred to column 3, lines 32-42, which make it clear that layers 22 and 32 are not epitaxial layers, but are like Sahara diffusions of dopants into epilayer 4.

With respect to claim 7, the Examiner suggests that Lee discloses the subject matter of claim 7 in "Figure 13B." Inasmuch as the Lee reference contains only Figures 1-4, applicants presume the Examiner intended to refer to Figure 2. As with the Sahara reference, there is no discussion or reference in the Lee patent which appears to disclose or relate to a logarithmic response to incident radiation.

Thus, in view of the above, the subject matter of claims 1 and 7 is not disclosed in the Lee reference either. As a result, any further rejection of claim 1 and 7 under §102 over either the Sahara or Lee reference is respectfully traversed.

Claim 2 stands rejected under 35 USC §103 as being unpatentable over Sahara or Lee as previously applied and further in view of Inoue. Inasmuch as claim 2 depends from claim 1, the above comments distinguishing claim 1 from

the Sahara and Lee references is herein incorporated by reference. The Examiner's admission that neither Sahara nor Lee teach "a substrate insulated from CMOS circuitry" is very much appreciated.

The Examiner contends that Inoue provides this missing teaching, suggesting that it would somehow be obvious to supply an insulated substrate as taught in Inoue. The Examiner is believed to be incorrect, as neither Sahara nor Lee indicate any need for an insulated substrate and Inoue is not concerned with photodiodes or associated read-out circuitry.

Other than the prohibited hindsight afforded by applicants' claimed invention, there is no reason to combine either Sahara or Lee with the Inoue reference. The Examiner has failed to establish any *prima facie* case of obviousness for applicants' claimed combination in view of the cited prior art and therefore has failed to meet the Patent Office's burden of establishing a *prima facie* case of obviousness.

Claims 3-6 stand rejected as unpatentable over Sahara or Lee and Inoue as applied to claim 2 and further in view of Cunningham et al. The above comments with respect to the Sahara or Lee references separately and in combination with the Inoue reference are herein incorporated by reference. While applicants have amended claim 3 in favor of newly written independent claim 38 (directed to the PIN embodiment) and claims dependent thereon, it should be noted that the Examiner admits that none of the three previously cited references disclose a photodiode being a PIN structure. Rather than picking and choosing bits and

pieces disclosed in a prior art reference, the Court of Appeals for the Federal Circuit has confirmed that the burden on the Examiner is to point out not only that the claimed structures are present in a plurality of prior art references, but that there is some reason or motivation for combining those references in the claimed manner.

Here the Examiner has provided no justification for combining the Sahara/Lee/Inoue combination with the Cunningham reference. Moreover, inasmuch as newly written claim 40 limits the subject matter of claims 38 and 39 to the epitaxial layer providing a high field region, this structure is clearly not shown in Cunningham, because he discloses a bulk wafer 22, which is not an epilayer, being the intrinsic or high field region (see Cunningham column 5, lines 47-48). As a result, any anticipated rejection of newly written claim 40 is respectfully traversed.

Claims 8 and 9 stand rejected under 35 USC §103 as unpatentable over Sahara or Lee as previously applied, further in view of Okabayashi. The above comments with respect to the Sahara and Lee references is herein incorporated by reference. The Examiner's admission that neither Sahara nor Lee teach "parasitic photo-diodes arranged to contribute to circuit output in response to incident radiation" is very much appreciated.

The Examiner contends that such structure is shown in Okabayashi and that it would be obvious to modify the Sahara or Lee references in such fashion. The parasitic photodiode PE_E of Okabayashi does not contribute to an output signal,

because it is merely a shunt across the power supply and ground connections (Vcc and GND).

Regarding claim 9, the Examiner admits that neither Sahara nor Lee teach the "amplifier arranged to provide feedback to stabilize photo-diode detector." The Examiner suggests that this is rendered obvious by the teaching in Okabayashi. Again, this is incorrect, because the amplifiers (AMP_A to AMP_D) merely amplifie signals from the photodiodes to generate outputs.

The Examiner has pointed to no feedback loop or circuit which controls photodiode current or voltage. Even if Okabayashi were combined with Sahara or Lee, it would not provide the claimed combination, and the Examiner has provided no reason why one of ordinary skill in the art would even try to combine the references. Therefore, the rejection of claims 8 and 9 over the Sahara or Lee references combined with Okabayashi is respectfully traversed.

Claim 10 stands rejected under 35 USC §103 as unpatentable over Sahara or Lee and Okabayashi as previously applied and further in view of Fossum. The above discussion on the Sahara/Lee and Okabayashi combination references is herein incorporated by reference.

The Examiner's admission that the Sahara/Lee and Okabayashi references fail to teach the claimed "load transistor" is very much appreciated. The Examiner then contends that it would be obvious to supply a load transistor as taught in Fossum. This is believed incorrect, as applicants claim the use of a load transistor in a feedback loop to stabilize the photodetector bias voltage. None of Sahara, Lee

or Okabayashi disclose such a feedback loop, so even if it were obvious to use a load transistor as taught in Fossum, there is no teaching to provide this as a feedback loop as recited in applicants' claims. Therefore, any further rejection of claim 10 is respectfully traversed.

Claim 11 is rejected under 35 USC §103 as unpatentable over Sahara/Lee and Okabayashi and Fossum as applied in claim 10 and further in view of Uchida. The above comments relating to the combination of references applied to claim 10 is herein incorporated by reference.

The Examiner admits that the combination of references applied in the rejection of claim 10 do not teach "the amplifier being a push pull amplifier." The Examiner contends that Uchida teaches a push pull amplifier. Because none of the references cited in claim 10 disclose a feedback loop, there is no reason to utilize a push pull amplifier for such a loop. Again, the Examiner is merely picking and choosing elements from various references utilizing applicants' claims as the basis for combining them in the fashion of the claim. Such is not the standard applied by the Court of Appeals for the Federal Circuit for judging the propriety of a rejection under 35 USC §103 and any further rejection thereunder is respectfully traversed.

Claim 12 stands rejected under 35 USC §103 as unpatentable over Sahara/Lee/Okabayashi/Fossum as applied in claim 10 and further in view of Kozlowski. The above comments regarding the cited references set out in claim 10 is herein incorporated by reference.

The Examiner again admits that the Sahara, Lee, Okabayashi and Fossum references all fail to disclose a "cascode transistor" and that it would be obvious to use such a transistor disclosed in the Kozlowski reference. Again, and as previously noted, such inclusion would be purposeless, because none of the Sahara, Lee, Okabayashi or Fossum references disclose an amplifier used in a feedback loop and therefore could not successfully incorporate a cascode transistor therein.

Furthermore, Kozlowski's teaching is to use a cascode transistor to increase gain and not for the effect of reducing Miller Effect capacitance in the manner that applicants employ such transistor. As a result, there is no support for the rejection of claim 12 and any further rejection thereunder is respectfully traversed.

Claim 13 stands rejected under 35 USC §103 as unpatentable over the Sahara/Lee references in further view of Inoue and Cunningham. Again, the above comments regarding the Sahara and Lee references, as well as the Inoue and Cunningham references, are incorporated by reference.

The Examiner's admission that Sahara and Lee do not teach "a substrate insulated from CMOS circuitry" is appreciated. The Examiner suggests that Inoue teaches that it would be obvious to combine such CMOS circuitry. However, the Examiner ignores the subject matter of claim 13, and it is noted that Inoue is not concerned with photodiodes or associated read-out circuitry and Cunningham does not disclose an undoped or intrinsic epilayer and instead teaches an undoped bulk wafer. Again, absent the hindsight afforded by applicants' claim, there is no

reason to combine Sahara or Lee with the bits recited in the Inoue and Cunningham references.

Claim 14 stands rejected over the Sahara or Lee references combined with Inoue and Cunningham as applied to claim 31 and further in view of Morikawa. Applicants can find no rejection of claim 31 contained in the Official Action and presumes the Examiner meant to refer to claim 13 and the reference to claim 31 is a typographical error. The above comments relating to Sahara or Lee in view of Inoue and Cunningham discussed in reference to claims 1 and 13 is herein incorporated by reference.

The Examiner's admission that none of these references teach "the undoped epitaxial layer being of SiGe alloy" and is very much appreciated. The Examiner suggests that Morikawa teaches the missing structure. While applicants do not claim that SiGe is novel per se, it is certainly novel when combined in the combination of elements set out in applicants' claim 14. The Examiner has provided no reason or basis for one of ordinary skill in the art to combine these references in the manner suggested. Accordingly, claim 14 is clearly patentable over the prior art.

As noted above, applicants have amended claim 1 to be directed primarily to the PN photodiode, with claims 2 and 4-14 dependent thereon and has added newly written claims 38-50 directed to the PIN embodiment. The dependency of those claims directed specifically to the PIN structure has been amended to reflect

the newly submitted claims. Consideration of newly submitted claims 38-50 is respectfully requested.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-50 remain in this application and are patentable over the cited prior art. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of these claims, he is respectfully requested to contact applicant's undersigned representative.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. *(Amended)* A photodetector circuit [including] comprising:

a photodiode detector, [(312/314)] said photodetector having a PN structure with p-type and n-type active regions; and

an associated readout circuit, [characterised in that the] said circuit incorporates a CMOS component [(300 to 312),] supporting at least one deposited epitaxial layer [(314)] which is [an] one of said active [region] regions of the photodiode detector and including a guard ring [(310)] delimiting and surrounding the photodiode detector [(312/314) to enhance] for enhancing electric field uniformity and [inhibit] inhibiting breakdown.

2. *(Amended)* A photodetector circuit according to Claim 1 [characterised in that] wherein the CMOS component comprises a substrate [(600)] supporting and insulated from said CMOS circuitry [(606)], the photodiode detector [(600/614/616/620)] is operable in current multiplication mode and the at least one epitaxial layer [(616)] is deposited upon the substrate [(600)].

3. *(Amended)* A photodetector circuit according to Claim [2 characterised in that the photodiode detector is a PIN structure (600/614/616/620) in which]39, wherein the at least one epitaxial layer [(616)] provides a high field region.

4. *(Amended)* A photodetector circuit according to Claim 2 [characterised in

that] wherein the photodiode detector is an avalanche photodiode [(600/614/616/620)] and said photodiode comprises a first region [(614)] incorporated in the substrate [(600)], and the at least one epitaxial layer is a layer [(616)] upon the first region [(614)] and provides a second region of the photodiode.

5. *(Amended)* A photodetector circuit according to Claim 2[characterised in that], wherein the at least one epitaxial layer comprises two layers [(616, 620)] providing second and third regions of the photodiode [(600/614/616/620)], the second region [(616)] is upon the first region [(614)] and the third region [(620)] is upon the second region [(616)], the first and third regions [(614, 620)] are of mutually opposite conductivity type, the second region [(616)] is substantially undoped and the third region [(620)] is an epitaxial layer.

6. *(Amended)* A photodetector circuit according to Claim 5[characterised],wherein in that the third avalanche photodiode region [(620)] is electrically connected to the guard ring [(612)] and has like potential therewith during circuit operation

7. *(Amended)* A photodetector circuit according to Claim 1 [characterised in that it is] arranged to provide a logarithmic response to incident radiation.

8. *(Amended)* A photodetector circuit according to Claim 1[characterised in that it], wherein said circuit incorporates parasitic photodiodes [(PPD21, PPD22)]

arranged to contribute to circuit output in response to incident radiation.

9. *(Amended)* A photodetector circuit according to Claim 1[characterised in that it], wherein said circuit includes an amplifier [(MA51/MA52)] arranged to provide feedback to stabilise photodiode detector bias voltage.

10. *(Amended)* A photodetector circuit according to Claim 9[characterised in that], wherein the amplifier [(MA51/MA52)] is arranged to amplify an output signal from the photodiode detector [(APD5)] and to provide feedback to bias a load transistor (ML5) in series with the photodiode detector [(APD5)].

11. *(Amended)* A photodetector circuit according to Claim 10[characterised in that], wherein the amplifier is a push-pull amplifier [(MA71/MA72)].

12. *(Amended)* A photodetector circuit according to Claim 10[characterised in that it], wherein said circuit includes a cascode transistor [(MC9)] arranged to reduce Miller Effect capacitance in the amplifier [(MA91/MA92)].

13. *(Amended)* A photodetector circuit according to Claim 1[characterised in that], wherein the CMOS component is a substrate [(600)] supporting and insulated from CMOS circuitry [(606)], the photodiode detector comprises a first region of one conductivity type [(614)] incorporated in the substrate, the at least one epitaxial layer comprises two epitaxial layers [(616, 620)] one of which [(616)] is substantially undoped and the other of which [(620)] is of opposite conductivity type to that of the first region [(614)], the first region [(614)] and the

two epitaxial layers [(616, 620)] being configured as a PIN diode.

14. *(Amended)* A photodetector circuit according to Claim 13[characterised in that], wherein the undoped epitaxial layer is of SiGe alloy or is a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes between successive layers.

--38. *(New)* A photodetector circuit comprising:

a photodiode detector, said photodetector having a PIN structure, said structure having three active regions, one region p-type, one region substantially undoped and one region n-type; and

an associated readout circuit, said circuit incorporates a CMOS component supporting at least one deposited epitaxial layer which is one of said active regions of the photodiode detector and including a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown.

39. *(New)* A photodetector circuit according to Claim 38 wherein the CMOS component comprises a substrate supporting and insulated from said CMOS circuitry, the photodiode detector is operable in current multiplication mode and the at least one epitaxial layer is deposited upon the substrate.

40. *(New)* A photodetector circuit according to Claim 39, wherein the photodiode detector is an avalanche photodiode and said photodiode comprises a first region incorporated in the substrate, and the at least one epitaxial layer is a layer upon the first region and provides a second region of the photodiode.

41. *(New)* A photodetector circuit according to Claim 39, wherein the at least one epitaxial layer comprises two layers providing second and third regions of the photodiode, the second region is upon the first region and the third region is upon the second region, the first and third regions are of mutually opposite conductivity type, the second region is substantially undoped and the third region is an epitaxial layer.

42. *(New)* A photodetector circuit according to Claim 41, wherein the third avalanche photodiode region is electrically connected to the guard ring and has like potential therewith during circuit operation.

43. *(New)* A photodetector circuit according to Claim 38, arranged to provide a logarithmic response to incident radiation.

44. *(New)* A photodetector circuit according to Claim 38, wherein said circuit incorporates parasitic photodiodes arranged to contribute to circuit output in response to incident radiation.

45. *(New)* A photodetector circuit according to Claim 38, wherein said circuit includes an amplifier arranged to provide feedback to stabilise photodiode detector bias voltage.

46. *(New)* A photodetector circuit according to Claim 45, wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor in series with the photodiode detector.

47. *(New)* A photodetector circuit according to Claim 46, wherein the amplifier is a push-pull amplifier.

48. *(New)* A photodetector circuit according to Claim 46, wherein said circuit includes a cascode transistor arranged to reduce Miller Effect capacitance in the amplifier.

49. *(New)* A photodetector circuit according to Claim 38, wherein the CMOS component is a substrate supporting and insulated from CMOS circuitry, the photodiode detector comprises a first region of one conductivity type incorporated in the substrate, the at least one epitaxial layer comprises two epitaxial layers one of which is substantially undoped and the other of which is of opposite conductivity type to that of the first region, the first region and the two epitaxial layers being configured as a PIN diode.

50. *(New)* A photodetector circuit according to Claim 49, wherein the undoped epitaxial layer is of SiGe alloy or is a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes between successive layers.--